IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT APPLICATION

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Applicant	:	Mark Visokay et al.	
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Commissioner for Patents
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2-15-2006

Jackie McBride

Jackie McBride

DECLARATION UNDER 37 C.F.R. 1.131

Sir:

YINGSHENG TUNG declares as follows:

1. THAT I am a legal representative of MARK VISOKAY and LUIGI COLOMBO in the subject application for Letters Patent;

2. THAT the applicants conceived the invention as set forth in the subject application for Letters Patent in the United States prior to September 18, 2003 and continually worked on the subject invention up to their reduction to practice as well as up to the filing of the instant application Serial No. 10/674,771, filed September 30, 2003, all in the United States;

3. THAT they reduced the invention to practice as disclosed in the subject application in the United States prior to September 18, 2003;

4. THAT all redacted dates on the attached pages of the invention disclosure are prior to September 18, 2003.

I declare under penalty of perjury that the above stated facts are true and correct on information and belief.

Yingsheng Tung

2-15-2006

Date

Respectfully submitted,

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TI-35943

Gate stack structure incorporating a single silicide for CMOS dual work function metal gates

Mark Visokay
Luigi Colombo

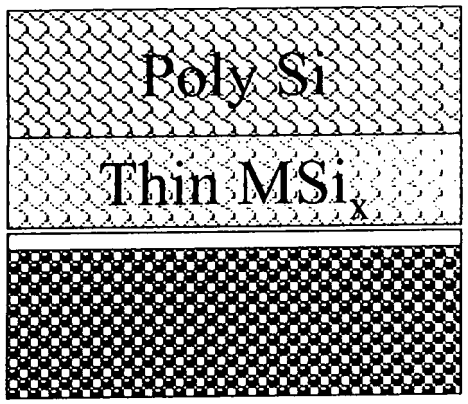
Background/problem statement

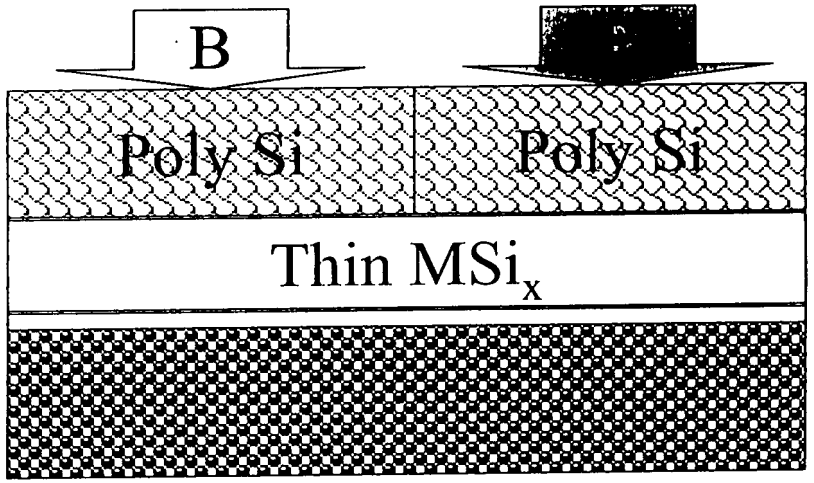
- It is desirable to replace poly-Si with metal gates in order to eliminate poly depletion, decrease Tox inversion and therefore improve drive current and performance.
- For CMOS metal gate technology, it is desirable to have tunable work functions (one value for NMOS and one for PMOS)
- Integration of two metals in a CMOS device is challenging from an integration perspective so it is desirable to use a single starting material and then modify it locally in the N & PMOS regions to provide differentiated work functions
- Channel engineering can be used to adjust the V_t for a midgap electrode, but this would be a difficult and risky channel engineering approach

Solution: e.g $MoSi_2$

- A representative stack would be 10 nm $MoSi_2$ under 70 nm poly-Si
- During the salicide loop, a NiSi layer would be formed on top of the poly-Si, allowing the gate sheet resistance spec to be met
- If desired, the $MoSi_2$ layer could be made thicker in order to allow consumption of all the poly-Si during the Salicide formation, thereby eliminating the poly-Si in the stack

Solution





MSi_x- is thermally stable on gate dielectric
M = W, Ta, Mo, Ti

Refractory silicides are etchable
WSi_2, $WSi_{2.x}$
$TaSi_2$, $TaSi_{2.x}$
$MoSi_2$, $MoSi_{2.x}$